a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

B'

Remarks

Claims 1-4 and 8-19 are pending in the instant application. Claim 1 has been amended a second time; the amendment has basis in the original specification.

Rejection under 35 U.S.C. §103

The Examiner has rejected claims 1-3, 8-10, 12 and 17 under 35 U.S.C. §103(a) as being unpatentable over Kabumoto in view of Parker et al. Applicants respectfully traverse this rejection. As noted in the previous response, this reference is concerned with a particular construction of ceramic package incorporating a power and ground plane. At column 3, lines 64 et seq., the insulating substrate is described as being formed of an electrically insulating material such as sintered aluminum oxide, aluminum nitride, sintered mullite, sintered silicone carbide or glass ceramic. The insulating substrate is prepared by producing a sludge of the powder of the raw material with an organic binder and making the sludge into sheets to provide a laminate of green ceramic sheets which is later fired at extremely high temperature. An insulating substrate formed from a polymeric compound loaded with high dielectric particles as is claimed in amended claim 1 is not contemplated, taught, nor suggested by the reference.

Further, although Kabumoto acknowledges the benefit of having capacitance (column 2, lines 14-18) within the package, he envisages a multi-layer capacitor (column 2, lines 21-32) which he discounts as being too bulky with the available dielectric constant of the substrate (column 2, lines 42-49). The patent then focuses on using these closely spaced planes as a low inductance path to the IC from an externally mounted chip capacitor (feature 9 in Figure 1). Kabumoto does not teach and will not produce significant capacitance from this internal plane

structure. The use of an external chip decoupling (column 5, lines 23-34) capacitor (typical value may be ~100 nanoFarrads) is acknowledgement of this fact.

The Examiner points out the existence of a capacitor between layers 10 and 11 in figure 1. Kabumoto does not "disclose" this as a capacitor but rather a low inductance plane pair. It is true that geometrically a capacitor would be generated although, as illustrated above, the capacitive value is too low to be useful. Given the geometry described in column 3, lines 24-28 and the dielectric constant of 7 (column 2, line 45), a capacitance per unit area of ~60 picoFarrad/cm^2 may be generated. This is three orders of magnitude less than the typical capacitance of an external chip capacitor, and therefore will provide a negligible improvement in the capacitive performance of the whole package.

Although Kabumoto illustrates the need for layers less than 0.1 mm to generate low inductance planes (column 6, lines 39-47), he does stress the difficulty in generating these thin layers. Given Kabumoto's recited manufacturing process, he proposes (column 4, lines 7-18) that anyone skilled in the art would recognize that the layer thickness must be limited to approximately 50 m in order to be handled. Taking this geometry into account, the capacitance generated would be about 120 pF/cm^2, which is still too small to have a significant effect on IC performance.

With regard to claim 3, the Examiner states that the heatsink (H) is synonymous with Applicants' stiffening member. Kabumoto teaches the use of the heatsink for its original intended purpose. He does not teach using the heatsink (H) as a stiffening member is not required in conjunction with a ceramic package. He also does not specifically teach that the heatsink must be metallic, although at the time that this patent was filed the majority of heatsinks were metallic although ceramic heatsinks were also available and now with recent advances filled polymeric heatsinks are now available.

With regards to claim 12, the Examiner states that the dielectric material includes a metal oxide. The package described in Kabumoto does indeed utilize sintered aluminum oxide as the dielectric material; the invention described by the Applicants detail the use of a dispersed metal oxide in a polymeric binder material. Further, the sintered aluminum oxide material described in Kabumoto does not have the required dielectric constant to be of use in Applicants' invention.

Parker discloses a high performance high-density integrated circuit component package having an IC chip with a plurality of IC bond pads and an interconnect substrate overlying the IC

chip. The interconnect substrate is formed from alumina and includes a separate layer of high dielectric constant materials. The combination of Kabumoto and Parker therefore at best discloses a package which is formed of ceramic or alumina, inorganic materials, which are not analogous to the nonconductive polymer substrate of Applicants' package which is filled with high dielectric particles. Such a construction would not be obvious to one skilled in the art from the combination of Kabumoto and Parker.

The Examiner has rejected claim 4 under 35 U.S.C §103 as being unpatentable over Kabumoto and Parker as applied to claims 1 and 3, and further in view of Dehaine et al. Kabumoto has been discussed above. Kabumoto combined with Parker and Dehaine does not render the claimed invention obvious. Dehaine discloses a package for very large scale integrated circuit which includes a ceramic interconnection structure (see e.g., column 3, lines 58-59) which is a multilayer block of ceramic. Therefore, the combination of Dehaine and Kabumoto discloses at most varying types of ceramic structures. Parker discloses an interconnect wherein the substrate is preferably alumina. (See column 5, lines 38-50.) A thin film of high dielectric such as tantalum oxide or barium oxide is included. A polymeric substrate filled with high dielectric constant particles is neither taught or suggested in any of the three references. Two references teaching only ceramic structures and a third teaching an inorganic substrate would not render such a construction obvious to one skilled in the art. Applicants therefore respectfully request that the rejection be withdrawn.

Claims 14-16, 18, and 19 are rejected as being unpatentable over Kabumoto and Parker et al. as applied and further in view of Fujisawa et al. Applicants traverse the rejection as it is not believed that any of these references disclose a package formed of a nonconductive polymer having an embedded capacitor. The arguments have been made for Kabumoto and Parker above, and because of the attached Affidavit under 37 C.F.R. §1.131, Fujisawa is not available as a reference for the claimed invention. Therefore, this rejection includes two references which disclose only ceramic or alumina substrates. Oxide layers are formed in Parker over the alumina substrate. There is no teaching or suggestion of a nonconductive polymeric substrate filled with high dielectric particles. Such a construction would not be obvious to one skilled in the art from the references. The Examiner is respectfully requested to withdraw the rejection.

The Examiner has further rejected claims 11 and 13 as being unpatentable over Kabumoto and Parker et al. as applied and further in view of Brandt et al.

First, Brandt does not render the claimed invention obvious. Brandt et al relates to a method of making discrete capacitors in a printed wiring board. A photodefinable insulator provides troughs to coat a capacitor dielectric therein-yielding separate capacitors. Whilst the current invention relates to one large shared capacitor in the structure, Brandt emphasizes the advantages of separate capacitors in design flexibility. The thickness of the photodefinable polymer is quoted at five microns at column 4, line 17.

Further, Brandt teaches away from coating large areas-large being defined as more than 0.25 cm^2. See, column 8, lines 8 to 23. Applicants teach capacitor areas of 7-10 cm^2. One skilled in the art would not find that the teachings of Brandt of small discrete capacitors in a printed wiring board would render obvious Applicants' package having a large shared embedded capacitor area. However, the above argument is rendered moot by the attached Affidavit under 37 C.F.R. §1.131, rendering Brandt unavailable as a reference. This leaves Kabumoto in view of Parker, which has already been discussed. Claims 11 and 13 require certain thicknesses and particular particles in the polymeric substrate. A nonconductive polymer substrate filled with dielectric particles is not taught nor suggested by the references. Specific particles for inclusion in the substrate are not taught nor suggested by the references. Applicants therefore respectfully request that the Examiner withdraw the rejection.

Applicants have earnestly tried to respond to each point raised by the Examiner in the official action. Applicants therefore respectfully request that the Examiner find all currently pending claims in condition for allowance.

Respectfully submitted,

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Version With Markings to Show Changes Made

1. An electronic package, comprising:

a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads;

a dielectric substrate mounted on the first side of the conductive trace layer made of a non-conductive polymer blended with high dielectric constant particles;

a capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm. including a first conductive layer, a second conductive layer and a layer of dielectric material disposed between the first and the second conductive layers, the first conductive layer mounted adjacent to the second side of the conductive trace layer;

a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.